APPENDIX A

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Pattern-Related Defects Become Subtler, Deadlier

Alexander E. Braun, Senior Editor – 6/1/2005
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At a Glance

With today's smaller geometries, any minor variation from the intended pattern, whether mask-induced or arising from the various other process steps, can assume catastrophic importance. Inspection for those defects is acquiring increasing importance, and requires rapid development of tool technology to detect and sort real defects from those that can be safely ignored.

Pattern-related defects can result from any anomaly, preventing the mask pattern from matching the intended pattern. Pattern imaging is based on direct imaging of the mask pattern and a comparison of the image either with design data, die-to-database inspection or another identical area of the mask.

"Pattern inspection has two key steps," said Franklin Kalk, CTO at Toppan Photomasks (Round Rock, Texas). "One is image acquisition, where the image of the pattern itself is acquired. The second is defect detection, where, after pattern image acquisition, it is interrogated for any anomaly that can be found." This provides defect location and rudimentary information about it, and then the information is fed to subsequent repair and/or defect review steps. Because the technique cannot reveal much about the defect itself, a review step is needed to understand more about it before attempting to repair it or deciding whether or not it will print on the wafer. Pattern inspection takes hours per mask, and the best tools have enough sensitivity to detect <100 nm defects.

Two technologies are used for image acquisition — high numerical aperture (NA) and aerial image inspection. The first consists of a high-NA microscope that detects variations from the intended pattern. It detects transmission deviation defects, such as a mouse-bite, line edge defect or a chrome spot; however, it does not do well with more advanced mask types, such as alternating phase-shift photomasks, where a quartz defect may exist.

Aerial image inspection mimics a wafer exposure tool and operates at a lower NA. Rather than directly imaging defects, it searches the pattern for variations from the intended CD. It is effective in detecting defects associated with phase anomalies. According to Kalk, the technique is useful for phase-shift masks. In principle, it can also verify defect printability. However, its sensitivity to the more classical defects is not as good as high-NA inspection.

High-NA tools work at longer wavelengths than those used by wafer exposure tools. State-of-the-art in wafer exposure is 193 nm, while high-end, high-NA tools operate at 257 nm. Thus, when a defect is found or a repaired defect is reviewed, there is a question about the defect or repair's printability since the tool does not operate at scanner wavelength. The aerial image approach operates at a scanner's wavelength, NA and illumination conditions. This provides more confidence on whether what is found is printable or not.

The main issues in photomask inspection center around pattern inspection. Generally, pattern inspection tools are not as reliable as the tools used for contamination inspection or inspection of photoblanks. Pattern inspection tools are complex, and can be the costliest single component of mass manufacturing. There are good reasons for this. The tools take longer to develop because they must be accurate, and it takes time to field one and verify that it provides the necessary data. Another consideration about pattern inspection tools is that generational changes, such as wavelength changes, are complicated. Interim upgrades can take longer to learn and be made to work well.

A closer integration of inspection into the manufacturing flow is indispensable — simple things like connection of the inspection data with defect review and repair. Defect review can be done with more insightful complementary techniques; SEM and μRaman techniques are excellent at reviewing defects and understanding more about them before deciding whether they should be repaired at all. Inspection data is now beginning to be fed into printability

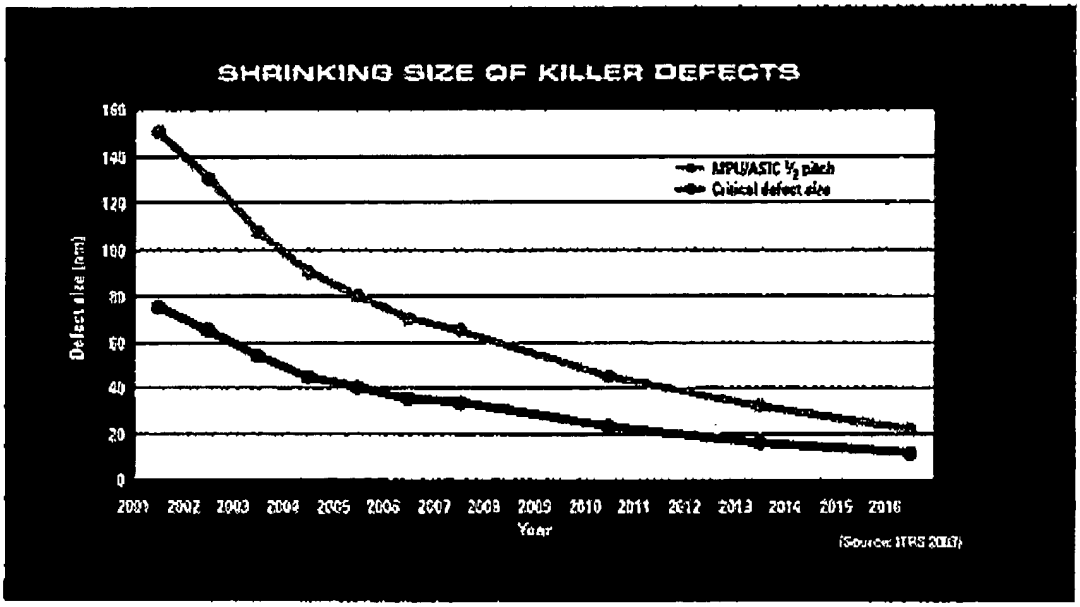
simulators.

The trend is toward intensive inspection of mask-critical areas. It is more cost-effective and faster to inspect areas where concern over defect printability is highest. Here, design for manufacturing (DFM) and design for yield (DFY) enter the picture, as an attempt is made to shift information up and down the engineering chain. It is becoming impossible to design in a vacuum, and the move is toward collaboration between designers since they generate the databases, the maskmakers who take the data and convert it into an actual physical object, and companies that build the inspection tools and printability simulators.

Nuisance or killer?

Although a high-NA tool is effective in finding pattern anomalies, it cannot distinguish between nuisance and real defects. For example, no feature on a mask has perfectly square corners. But if the corner rounding varies too much, the wafer print may be unfaithful to the original design. However, it is difficult to modulate pattern inspection tools' sensitivity to these subtle variations.

To detect critical defects, the tool must run at high sensitivity and the algorithms might still not distinguish between subtle variations that matter and those that do not. An inspection may find 1000 defects on a mask, of which only three really count (Fig. 1).



1. As defects — nuisance and real — get smaller, inspection platforms must fight back with higher sensitivity. Since this tends to lead to the detection of hundreds of nuisance defects, more computing power and increasingly sophisticated algorithms are required to cull them out. At 45 nm, both high sensitivity and higher throughput will be required. (Source: Applied Materials)

Ehud Tzuri, global product manager for wafer inspection products at Applied Materials (Rehovoth, Israel), observed that 65 nm defects repeat in advanced work. "We're seeing small and shallow voids, 20 to 30 nm, in STI layers," he said. While there are always bridge-type defects in metal lines and footers — residues at the bottom of poly lines — device makers are also getting defects such as partially closed single contacts. Then there are high-aspect-ratio defects inside trenches and vias, which are smaller, more critical, and complicated to inspect. A 30 nm void in a 130 nm design rule was a nuisance defect; now at 65 or 45 nm, it can be a killer defect.

Smaller defects require higher inspection sensitivity, which sometimes leads to high numbers of nuisance defects on certain layers. Nuisance defects must be culled from those of importance during inspection. Since sensitivity is

often obtained at the throughput's cost, this creates another hurdle. At 45 nm, throughput must increase dramatically if technologies such as brightfield inspection are to be used as production-worthy inspection resources. This will require additional computing power, more sophisticated algorithms, and changes in the brightfield optical technology itself. Traditionally, brightfield inspection has depended upon lamp-based microscopy, which limits usable light. Resolution is obtained by illuminating the wafer with a small spot and collecting the reflected light at the brightfield angle. Lamp-based brightfield technology has inherently limited illumination levels, which results in insufficient detection sensitivity on materials that are damaged by light or are not very reflective. "Current systems operating at 65 nm are extendable," Tzuri said. "At 45 nm, we'll probably inspect for 20 nm defects, and at that node, brightfield will be used in production."

Reticles and marginalities

Anantha Sethuraman, vice president of product marketing at FEI Co. (Hillsboro, Ore.), has seen pattern-related defectivity mechanisms change. "The worst pattern-related defectivity occurs both at the front and back end — in the front end because of the proximity correction and reticle enhancement techniques (RETs) related issues of transistor structures, and in the back end due to tighter design rules and high-aspect-ratio-induced complications," he said. Pattern-transfer defectivity impacts not only yield, but also the DFM framework. The industry expects existing lithography platforms to print finer lines without spending on new mask designs, so RETs were designed. However, in many of these layers, RETs must be employed less, and more intelligently.

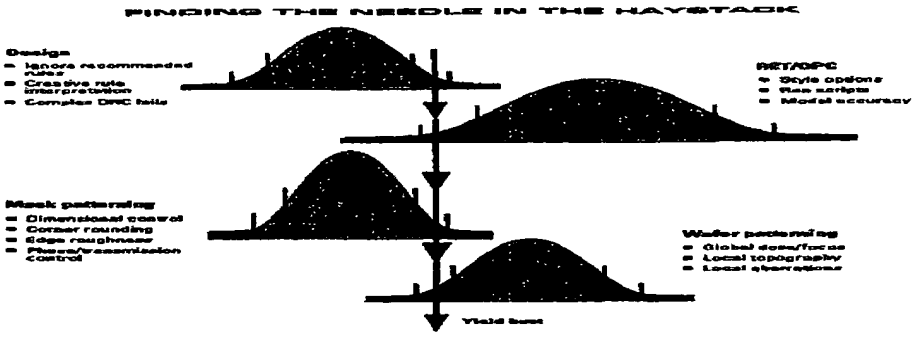
Rule-based RET definitions are used; however, when the process goes from translating a sharp angle from the design's OPC side to printing it on the wafer, corners are rounded and lines are close together, and it is possible to go only so far in separating them and putting design rules or restrictions on the separating distances. If lines are improperly defined or separated, bridging issues result, because there is little oxide between individual lines in the back end. These issues are troublesome to various modules — not just interconnect — in other areas of chip fabrication. Thus, pattern-related defectivity is not just connected to pattern, but to design, printing, and its definition. Wherever one turns, whether it be to EDA space, lithography or etch, issues are being created.

Systematic defects increase

According to Ingrid Peterson, senior technical director, and Sagar Kekare, senior applications development manager, at KLA-Tencor (San Jose), the systematic component of the defect distribution, as opposed to the random component, is becoming increasingly important. "IC manufacturing is struggling more with systematic defects, which occur in the same pattern area of the chip," said Peterson, adding that a survey revealed the wafer fab module that mainly contributes to these systematic defects is lithography, followed by etch, and then CMP.

Kekare pointed out that, two generations ago, pattern defects meant extra or missing resist in unexpected places. "Today, there's a sense of expectation on the part of the lithography and mask-shop engineers about which pattern configurations will have issues and which will pass," he said. Yet, some pattern configurations appear in a new design without warning and are difficult to handle, because the data that goes to the mask shop is heavily decorated. Lithography module issues have a devastating carry-forward effect; the way small gaps are defined at the lithography step and later, how film deposition fills these gaps, can lead to buried voids and other factors that alter the dielectric constant locally. This, in turn, throws off calculations and models made about parallel interconnect lines, introducing errors in the electrical libraries pertaining to interconnects. Alternately, if CMP opens up these voids, they may fill up with the conducting layer, producing a bridge and subsequently shorted interconnects.

These are not systematic defects originating from reticle imperfections. They arise from the interaction of the complexity of the RETs with the layout, mask manufacturing, and finally with wafer processing. Even a slight marginality that is still within the specification limits can — when combined with subsequent steps — cause catastrophic failures. If several steps in the flow fall at the edge of the statistical distribution rather than dead center, they can stack up like blocks, resulting in a catastrophic failure or yield bust at the wafer level. In the past, marginalities were easy to characterize through discrete measurements across the die. The lithography process window would be characterized using a CD-SEM, and CDs would be measured at specific locations. Subsequently, etch-rate measurements would be performed at dense and isolated areas to determine effects like microloading. Today, no one really knows where marginalities will occur. There are in-between spaces, or in-between configurations or patterns, which are likely to be more susceptible than the sampling points chosen to define the process window. These marginalities or needle-in-a-haystack features can severely restrict the process window, and a failure may remain unnoticed until electrical test (Fig. 2).



2. If several steps in the design to OPC to maskmaking to wafer processing flow fall at the edge of the statistical distribution rather than dead center, they can build up, resulting in a catastrophic failure or yield bust. (Source: KLA-Tencor)

At electrical test, the first screening gives a broad idea of a failure; further pinpointing it to a specific patterning issue can take several iterations of increasingly complex tests. As a result, it might take up to three months from the time the reticle with the marginality enters the fab and starts producing wafers before the root causes of the failure is determined. KLA's solution to finding these marginalities is called process window qualification (PWQ), which can reduce this process to a couple of days by identifying the marginal feature when the reticle enters the fab prior to producing product. "One of our customers cited that, once the usual tests are performed throughout the design to OPC to maskmaking to wafer processing flow, PWQ is the last line of defense before their new mask set is released," Kekare said.

Looking at mask verification

According to Patrick Martin, executive director of core technology at Photronics (Allen, Texas), there are limitations in inspection. "One is that we use an off-actinic inspection system, based on a split-frequency laser, with an inspection wavelength of 257 nm." The patterning requirements for applications at ≤90 nm have lithography requirements that drive a 193 nm source. "With inspection capability set for 257, we're troubled about material properties and specifically missing defects that could be opaque at 193 but transmissive at 257 nm," he said. There is concern about the capability to detect defects with material properties that are actinic, or 193 nm

specific. That is true for both phase- and transmission-related defects, making it a major mask verification challenge.

At 45 nm, another challenge is two- and three-dimensional mask measurements. To obtain an indication of the mask feature area's fidelity, flux was measured to determine how an aerial image actually transfers down to the wafer. In addition, 3-D-related effects, such as sidewall and phase-type configuration measurements, are being made to understand the sensitivity of these masks' characteristics to wafer-level performance. In terms of pattern-related defects, pinhole detection is an isue. Detecting small pinholes that can image at 193 nm — especially in phase-shift applications — may be difficult. Then there is complementary phase-shift technology requiring alternating aperture phase-shift masks, and the capability to detect phase defects and other defects close to the pi shifter boundaries; there is a limitation there, especially if it is in undercut-related configurations for intensity balancing.

Achieving an actinic inspection system presents problems. There are engineering obstacles, and the consumables are expensive. There are not many of these systems to address 45 nm applications, and with roughly a dozen companies on the planet working on 45 nm, there seems to be an entry barrier below 90 to 65 and 45 nm, since the tools will probably be prohibitively expensive.

Edging toward integrated metrology

Sanjay Yedur, product marketing manager at Timbre Technologies (Santa Clara, Calif.), has evidence that optical digital profiling (ODP) has value as a non-destructive, production-worthy CD and profile measurement tool for wafer and mask applications. Profile information is critical in mask wet-etch processes where undercut underneath the chrome is prevalent, as well as in advanced phase-shift masks. When coupled with spectra obtained from a Nanometrics Atlas-M system, ODP provides reliable CD, sidewall angle and etch depth on masks. CD and profile metrology is critical, as top-down information generated by the CD-SEM is no longer sufficient for advanced mask features. ODP overcomes the issues inherent in conventional CD-SEM, such as charging and LER. It can also confirm features appearing as a result of improper processing, such as over or underetching.

"The size and speed of optical profiling opens up the possibility of integrating the metrology," Yedur said. The efficiencies of integrated metrology suggest that it will be implemented to replace standalone tools in the fab. An immediate result of this is that it will become possible to get CD and profile data for the entire reticle or wafer within a short period of time. When this happens, manufacturing control and processing fault-detection strategies that were unavailable before can be put into place.

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